Remarks

Entry of this amendment and allowance of all claims are respectfully requested. Claims 1-35 remain pending.

In accordance with 37 C.F.R. 1.121(c)(1)(ii), a marked-up version of the amended claims is provided on one or more pages separate from the amendment. These pages are appended at the end of the Response.

By this paper, applicants amend claims 1, 2, 9, 16, 17, 27 & 32-35 to more clearly point out and distinctly claim certain features of applicants' invention. Specifically, applicants delete herein the phrase "real time" when used in connection with applicants' continuously obtaining the fullness of the external buffer. This amendment to the claims constitutes a bona fide attempt by applicants to advance prosecution of this application by refocusing attention to certain remaining recited subject matter. It is believed that the amendments to the claims place all claims in condition for allowance.

In the Office Action, claims 1-6, 16-19, 32 $ 34 were rejected under 35 U.S.C. 102(e) as being anticipated by Greenfield et al. (U.S. Patent No. 5,760,836), while claims 7-15, 20-31, 33 and 35 were rejected under 35 U.S.C. 103(a) as being unpatentable over Greenfield et al. further in view of Choe et al. (U.S. Patent No. 6,094.696). Applicants respectfully, but most strenuously, traverse these rejections and request reconsideration.

As is well known, there is no anticipation of a claim unless (1) all the same elements are (2) found in exactly the same situation and (3) are united in the same way to (4) perform the identical function. In this case, the encoding techniques of Greenfield et al. clearly do not have the same elements, nor are they capable of being readily modified to include the same elements, as that recited by applicants in independent claims 1 & 16.

Applicants recite in these independent claims a technique for encoding a digital video image stream in an encoder. The technique includes feeding back to hardware logic within the encoder an external buffer read signal from a host and incrementing an on-chip counter of the hardware logic each time that the external buffer is read, and counting therefrom the number of bits read by a host (R). The technique further includes determining the number of bits encoded and written into an external buffer (E), and in hardware logic of the encoder subtracting from a number of bits encoded (E) the number of bits read by the host (R) to continuously obtain the fullness of an external buffer (BF). The technique further includes providing, from the hardware logic of the encoder to the host, a dynamic buffer level indicator in real time indicative of the fullness of the external buffer (BF).

Dependent claims 32-35 further recite that the continuous updating comprises obtaining the fullness of the external buffer (BF) every cycle of the encoder.

To restate, the present invention employs hardware to continuously monitor the real time fullness of the external buffer and provide a dynamic buffer level indicator indicative of the fullness of the external buffer. This dynamic buffer level indicator assists the host's application and the control of reading compressed data from the external buffer coupled to the encoder. The buffer level indicator is dynamic in that the indicator is adjusted based on continuous monitoring of the external buffer, e.g., every cycle of the encoder. (See page 4, lines 26-33).

In support of the anticipation rejection, the Office Action alleges the teachings at columns 5-7 of Greenfield et al. as reciting the above-summarized aspects of applicants' invention. This characterization of the teachings of Greenfield et al. is respectfully traversed. In support of this traversal and the following comments, applicants wish to note the significant overlapping in inventorship between the present application and the inventors of the Greenfield et al. patent. Applicants are well aware of the teachings and capabilities of the system described in Greenfield et al. and note the following differences between that system and the present technique.

Applicants respectfully submit that a careful reading of Greenfield et al. fails to uncover any teaching, suggestion or implication that the processing or logic described therein comprises a dynamic buffer level indicator that is provided as recited by applicants herein. In fact, Greenfield et al. specifically describes a non-real time

buffer level indicator. In Greenfield et al. the buffer level indicator is provided dependent upon how often the processor updates the indicator. The hardware described in Greenfield et al. would be incapable of supporting a continuously obtaining application as recited herein. Column 6, lines 18-29 specifically state that the microcode reads the register and compares it with the buffer fullness in bytes (BF/8). This means that the processor is doing the updating of the buffer level indicator and that the buffer level signal is not returned on a continuous basis. As one example, in the Greenfield et al. system, a buffer level indicator would be returned approximately once per picture frame. In contrast, applicants' hardware logic continuously obtains the fullness of the external buffer. In claims 32-35 this continuous obtaining is recited to occur with every cycle of the encoder, which is clearly incapable with a system such as described by Greenfield et al.

As noted at page 14 & 15 of applicants' specification, the disadvantage of the above-summarized approach (i.e., the Greenfield et al. approach) is that it is implemented in microcode, and therefore, buffer fullness in not constantly monitored. Without a continuous view of the fullness of the buffer, the host processor must wait until the microcode goes in, polls the on-chip register and calculates the fullness of the FIFO. This creates a latency issue which produces an inherent inaccuracy in the FIFO fullness reading.

The present invention solves this problem by implementing FIFO monitoring and a dynamic FIFO buffer level indicator in hardware logic inside the digital video encoder for interfacing, for example, to an industry standard FIFO buffer or cascaded FIFO buffers. Thus, applicants continuously attain the recited dynamic buffer level indicator through the use of a hardware implementation. Clearly, Greenfield et al. describes a microcode implementation, which, based on the processing described therein, comprises a non-continuous implementation. This is understood by one skilled in the art through the use of a non-real time counter to monitor the amount of data written to the FIFOs in Greenfield et al. (see column 6, lines 10-11), and through the use of a non-continuous sampling of this counter by the microcode.

Responsive to the Examiner's comments contained at page 6, line 7 - page 7, line 6 of the Office Action, applicants note that column 1, lines 37-49 and column 5, lines 24-30 each discuss a real time encoder. However, neither of these columns teaches, suggests or implies a continuous monitoring of external buffer fullness as recited in the independent claims presented herewith. Real time encoding is different from and independent of applicants' recited continuous monitoring of external buffer fullness. As noted above, the monitoring of external buffer fullness in Greenfield et al. is necessarily non-continuous based upon the teachings set forth therein. **In fact, the present invention arose from applicants' identifying of the deficiency of the Greenfield et al. teachings in this respect.** The formulas set forth in

Greenfield et al. clearly indicate to one skilled in the art that the processor determination of buffer level fullness described therein is a non-continuous calculation. To further recite the difference, applicants point to claims 32-35 wherein the continuously obtained fullness of the external buffer is determined every cycle of the encoder, i.e., every machine cycle. This is distinct from any teaching, suggestion or implication in Greenfield et al.

In view of the above, applicants respectfully submit that there are clear differences between the encoding technique recited in claims 1 & 16 and the teachings, suggestions or implications in Greenfield et al. Therefore, applicants request withdrawal of the anticipation rejection and allowance of independent claims 1 & 16, as well as the claims which depend therefrom.

As noted, claims 7-15, 20-31, 33 & 35 were rejected under 35 U.S.C. 103(e) as being unpatentable over Greenfield et al. further in view of Choe et al. This rejection is respectfully traversed.

An "obviousness" determination requires an evaluation of whether the prior art taken as a whole would suggest the claimed invention taken as a whole to one of ordinary skill in the art. In evaluating claimed subject matter as a whole, the Federal Circuit has expressly mandated that functional claim language be considered in evaluating a claim relative to the prior art. Applicants' respectfully submit that the application of these standards to the

independent claims presented herewith leads to the conclusion that the recited subject matter would not have been obvious to one of ordinary skill in the art based on the applied patents.

Assuming, arguendo, that the combination is proper, the combination fails to teach or suggest certain features of the claimed invention. For example, each independent claim at issue (i.e., claims 9 & 27) recites a technique wherein hardware logic within the encoder continuously obtains and provides to the host a dynamically updated flag. Neither Greenfield et al. nor Choe et al. continuously obtain and provide from encoder hardware to a host a dynamically updated flag. In fact, applicants note that Choe et al. does not even involve an encoding process.

As noted above, a careful reading of Greenfield et al. fails to uncover any teaching, suggestion or implication of hardware logic implementing a technique wherein a dynamic buffer level indicator is continuously obtained and provided to a host. Similarly, a careful reading of Choe et al. fails to uncover any discussion of an encode process, let alone the provision of a dynamic buffer level indicator from an encoder to a host. In fact, a careful reading of Choe et al. fails to uncover any dynamic indicator being continuously provided, as disclosed in the present application. Choe et al. disclose a data transfer mechanism where a set of buffer_full and buffer_empty flags are implemented for each device. Once a flag is set it has to be reset by the CPU. This is in contrast with the flags

disclosed by applicants which are dynamic, real time indicators. As the data is added to the pre-defined full level the buffer_full flag is asserted in applicants' case. Further as data is removed to below the pre-defined full level, the buffer_full flag is deasserted without any CPU intervention. The flags of Choe et al. are used to start data transfer operations. In contrast, the flags recited by applicants do not necessarily initiate data transfer. Applicants flags are used to regulate the data rate in and out of the FIFOs in a simultaneous and continuous manner.

For all the above reasons, applicants respectfully submit that independent claims 9 & 27 would not have been obvious to one of ordinary skill in the art based upon Greenfield et al. and Choe et al. In applicants' recited invention, hardware logic within the encoder performs certain functions, including subtracting from a number of bits encoded the number of bits read by the host to continuously obtain the fullness of an external buffer. Further, from this hardware logic, a dynamically updated flag is provided in real time to a host. Since applicants' invention is implemented within hardware logic within the encoder, no CPU intervention is required. In fact, only with a hardware implementation is it possible to obtain applicants' recited continuously obtaining the fullness of the external buffer and providing in real time the dynamically updated flag.

The dependent claims are believed allowable for the same reasons as the independent claims, as well as for their

own additional characterizations. For example, claims 33 & 35 recite that the hardware logic continuously obtains the fullness of the external buffer every cycle of the encoder. A careful reading of the applied art fails to uncover any suggestion or capability that the systems described therein could obtain every cycle of the encoder the fullness of the external buffer. In fact, this is simply not possible using a CPU based system such as described by Greenfield et al. and Choe et al.

In view of the above Amendments and Remarks, applicants respectfully request allowance of all claims pending herein. Should the Examiner wish to discuss the case with applicants' attorney, please contact applicants' attorney at the below listed number.

Respectfully submitted,

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Marked-Up Version of Claims

Kindly amend claims 1, 2, 9, 16, 17 27 & 32-35 as set forth below.

1. (Thrice Amended) In a method of encoding a digital video image stream in an encoder, comprising spatial compression of still images in the digital video image stream and temporal compression between the still images, wherein the spatial compression is carried out by converting a time domain image of a macroblock to a frequency domain image of the macroblock, taking a discrete cosine transform of the frequency domain image, transforming the discrete cosine transformed macroblock image by a quantization factor, and run length encoding the quantized discrete cosine transformed macroblock image, wherein the temporal compression is carried out by reconstructing the quantized, discrete cosine transformed image of the macroblock, searching for a best match macroblock, and constructing a motion vector therebetween, to thereby form a bitstream comprising run length encoded, quantized, discrete cosine transformed macroblocks and motion vectors, and passing the bitstream to and through an external buffer to a transmission medium, the improvement comprising feeding back to hardware logic within the encoder an external buffer read signal from a host and incrementing an on-chip counter of the hardware logic each time that the external buffer is read and calculating therefrom the number of bits read by a host (R), and determining the number of bits encoded and written into an external buffer (E), and in the hardware

logic of the encoder subtracting from a number of bits encoded (E) the number of bits read by the host (R) to continuously obtain the [real time] fullness of an external buffer (BF), and providing, from the hardware logic within the encoder to the host, a dynamic buffer level indicator in real time indicative of the fullness of the external buffer (BF).

2. (Thrice Amended) The method of claim 1, wherein said providing the host with said dynamic buffer level indicator comprises continuously comparing the [real time] fullness of the external buffer (BF) with a buffer threshold (BT) defined by said host and providing a high-level indicator when a buffer fullness (BF) is greater than the buffer threshold (BT), and a low-level indicator when the buffer threshold (BT) is greater than the buffer fullness (BF).

9. (Thrice Amended) In a method of encoding a digital video image stream in an encoder, comprising spatial compression of still images in the digital video image stream and temporal compression between the still images, wherein the spatial compression is carried out by converting a time domain image of a macroblock to a frequency domain image of the macroblock, taking a discrete cosine transform of the frequency domain image, transforming the discrete cosine transformed macroblock image by a quantization factor, and run length encoding the quantized discrete cosine transformed macroblock image, wherein the temporal compression is carried out by reconstructing the quantized,

discrete cosine transformed image of the macroblock, searching for a best match macroblock, and constructing a motion vector therebetween, to thereby form a bitstream comprising run length encoded, quantized, discrete cosine transformed macroblocks and motion vectors, and passing the bitstream to and through an external buffer to a transmission medium, the improvement comprising feeding back to hardware logic within the encoder an external read signal from a host and incrementing an on-chip counter of the hardware logic each time that the external buffer is read and calculating therefrom the number of bits read by a host (R), and determining the number of bits encoded and written into an external buffer (E), and in the hardware logic of the encoder subtracting from a number of bits encoded (E) the number of bits read by the host (R) to continuously obtain the [real time] fullness of an external buffer (BF), and providing, from the hardware logic within the encoder to the host, in real time a dynamically updated flag comprising at least one of a BUFFER_EMPTY flag, a BUFFER_ALMOST_FULL flag and a BUFFER_FULL flag.

16. (Thrice Amended) An encoder for encoding a digital video image stream in the encoder, comprising means for spatial compression of still images in the digital video image stream and means for temporal compression between the still images, wherein the means for spatial compression comprises means for converting a time domain image of a macroblock to a frequency domain image of the macroblock, means for taking a discrete cosine transform of the frequency domain image, means for transforming the discrete

cosine transformed macroblock image by a quantization factor, and means for run length encoding the quantized discrete cosine transformed macroblock image, wherein the means for temporal compression comprises means for reconstructing the quantized, discrete cosine transformed image of the macroblock, means for searching for a best match macroblock, and means for constructing a motion vector therebetween, said encoder for encoding a digital video image stream thereby forming a bitstream comprising run length encoded, quantized, discrete cosine transform macroblocks and motion vectors and passing the bitstream to and through an external buffer to a transmission medium, the improvement comprising means for feeding back to hardware logic within the encoder an external read signal from a host, and for incrementing an on-chip counter of the hardware logic each time that the external buffer is read and calculating therefrom the number of bits read by a host (R), said hardware logic in the encoder being further adapted to monitor a number of bits encoded (E) and written into the external buffer and subtract from the number of bits encoded (E) the number of bits read by the host (R) to continuously obtain the [real time] fullness of an external buffer (BF), and wherein said hardware logic in the encoder is further adapted to provide the host with a dynamic buffer level indicator in real time indicative of the fullness of the external buffer (BF).

17. (Thrice Amended) The encoder of claim 16, wherein said logic adapted to provide the host with a dynamic buffer level indicator comprises logic adapted to continuously

compare the [real time] fullness of the external buffer (BF) with a buffer threshold (BT) defined by said host and to provide a high-level indicator when a buffer fullness (BF) is greater than the buffer threshold (BT), and a low-level indicator when the buffer threshold (BT) is greater than the buffer fullness (BF).

27. (Thrice Amended) An encoder for encoding a digital video image stream in the encoder, comprising means for spatial compression of still images in the digital video image stream and means for temporal compression between the still images, wherein the means for spatial compression comprises means for converting a time domain image of a macroblock to a frequency domain image of the macroblock, means for taking a discrete cosine transform of the frequency domain image, means for transforming the discrete cosine transformed macroblock image by a quantization factor, and means for run length encoding the quantized discrete cosine transformed macroblock image, wherein the means for temporal compression comprises means for reconstructing the quantized, discrete cosine transformed image of the macroblock, means for searching for a best match macroblock, and means for constructing a motion vector therebetween, said means for encoding a digital video image stream thereby forming a bitstream comprising run length encoded, quantized, discrete cosine transform macroblocks and motion vectors and passing the bitstream to and through an external buffer to a transmission medium, the improvement comprising means for feeding back to hardware logic within the encoder an external read signal from a host, and for

incrementing an on-chip counter of the hardware logic each time the external buffer is read and calculating therefrom the number of bits read by a host (R), said hardware logic in the encoder being further adapted to monitor a number of bits encoded (E) and written into the external buffer and subtract from the number of bits encoded (E) the number of bits read by the host (R) to continuously obtain the [real time] fullness of an external buffer (BF), and wherein said hardware logic in the encoder is further adapted to provide the host in real time with dynamically updated flags comprising a BUFFER_EMPTY flag, a BUFFER_ALMOST_FULL flag and a BUFFER_FULL flag.

32. (Amended) The method of claim 1, wherein the continuously obtaining comprises obtaining the [real time] fullness of the external buffer (BF) every cycle of the encoder.

33. (Amended) The method of claim 9, wherein the continuously obtaining comprises obtaining the [real time] fullness of the external buffer (BF) every cycle of the encoder.

34. (Amended) The encoder of claim 16, wherein the hardware logic continuously obtains the [real time] fullness of the external buffer (BF) every cycle of the encoder.

35. (Amended) The encoder of claim 27, wherein the hardware logic continuously obtains the [real time] fullness of the external buffer (BF) every cycle of the encoder.